ISSN 2349-7815

International Journal of Recent Research in Electrical and Electronics Engineering (IJRREEE)
Vol. 4, Issue 2, pp: (46-52), Month: April - June 2017, Available at: www.paperpublications.org

Interleaved Boost Converter with Cumulative Voltage Unit

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Abstract: **A boost converter is a DC to DC converter with an output voltage greater than the source voltage. But it produces large input current ripple. In order to improve the efficiency of the boost converter and reduce the ripple current, an interleaved boost converter is used. An interleaved boost converter consists of several boost converters connected in parallel with switching frequency and a phase shift of 180˚. A new interleaved high step-up DC-DC converter with the circuit of cumulative voltage unit (CVU) is presented in this work. This converter is suitable for the high gain applications. Only two switches are required to form the boosting path and the interleaved topology. Each CVU module can share common diodes to reduce the number of the components and step up the voltage gain. The interleaved structure in the input end can reduce the power loss in each current-owing component and the input current ripple. The interleaved boost converter with voltage summation unit can be verified by using MATLAB/SIMULINK.**

Keywords: **Cumulative voltage unit, Boost converter, Interleaved boost converter, Voltage Stress.**

I. INTRODUCTION

In recent years, due to the fast environmental change and energy exhaustion, the application ranges of the renewable energy is extended more and more. The DC-DC step-up converter is one of the possible applications. In general, the voltage generated from the green energy is through the DC-DC converter to step up the voltage [6]. However, the renewable energy such as fuel cell, solar system, and wind power will not generate an enough high voltage. A conventional boost converter, the stray inductance, capacitor, voltage stress, ESR of the capacitor and reverse recovery problem of the diode make it cannot produce the necessary high voltage in the real applications. The duty cycle of the conventional boost converter has its limitation to step up the output voltage [6]. A new interleaved high step-up dc-dc converter with the circuit of cumulative voltage unit is used for high power applications. Only two switches are required to form the double boosting path and the interleaved topology. The new technique of the cumulative voltage unit forms the post part of the high step-up converter[6]. Each CVU module can share common diodes to reduce the number of the components, step up the voltage gain and clamp the voltage effectively. The interleaved structure in the input end can reduce the power loss in each current-owing component and the input current ripple.

II. INTERLEAVED BOOST CONVERTER WITH CUMULATIVE VOLTAGE UNIT

The high gain interleaved boost converter is suitable to the application of requiring high ratio of the output voltage to input voltage. Only two switches are required to form the double boosting path and the interleaved topology. The new technique of the cumulative voltage unit forms the post part of the high step-up converter. Each CVU module can share common diodes to reduce the number of the components, step up the voltage gain and clamp the voltage effectively. The interleaved structure in the input end can reduce the power loss in each current-owing component and the input current ripple. The CVU modules can be arranged with different manners to extend the circuit topology. A boost converter is not

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suitable for high power applications. The main drawbacks are the stray inductance, input current ripple, voltage stress, equivalent series resistance of the capacitor, and reverse recovery problem of the diode. These drawbacks make it not suitable to produce the necessary high voltage in the real applications. The duty cycle of the conventional boost converter has its limitation to step up the output voltage. Single input path of the conventional boost converter makes the input ripple current be larger and the power loss can also be larger. So, interleaved boost converter can be used for ripple reduction and to reduce the size and thus rating of the components. Conventional boost converter and interleaved boost converters have some common drawbacks. The duty cycle of the these boost converters has its limitation to step up the output voltage. For high power applications it require large value of duty cycle. Extreme value of duty cycle is affected by the design of circuit. The voltage stress across the switch is almost equal to output voltage in both cases. Therefore it is necessary to provide high output voltage at small value of duty cycle with low ratings of components which helps to reduce the size of the circuit. Figure 1 shows the circuit diagram of Interleaved Boost Converter with Voltage Cumulative Unit.

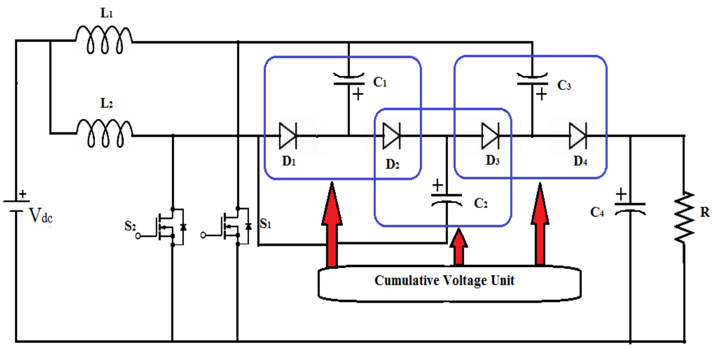


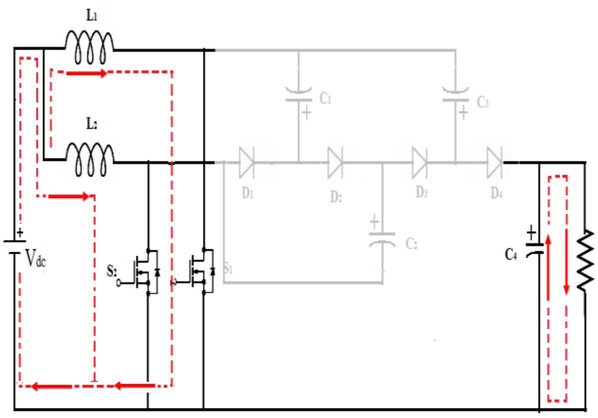
Fig.1. Circuit diagram of Interleaved Boost Converter

A. Modes of Operation:

The circuit is operated at the condition that the duty cycle is greater than 0.5. When the duty cycle is smaller than 0.5, it can also be operated but the voltage gain is decreased. However, the application of high voltage gain makes the proposed circuit be operated at D should be greater than 0.5 in general. In one cycle, the circuit owns four operating modes. The driving signals of switches S_1 and S_2 are 180˚ phase shifted.

(a). Mode 1$[t_0 - t_1]$

The switches S_1 and S_2 are in conduction. As shown in figure 2, the inductors L_1 and L_2 store the energy form the input side. All diodes are in the off state. The rectifier D_1 must sustain the voltage of C_1. The rectifiers D_2, D_3, and D_0 must sustain the voltage difference between the before-capacitor and the after capacitor of their positions. The circuit will enter mode 2 when the switch S_2 is turned off. Figure 3 shows the theoretical waveforms of Interleaved boost converter with cumulative voltage unit.Shaded potion shows mode 1 operation.



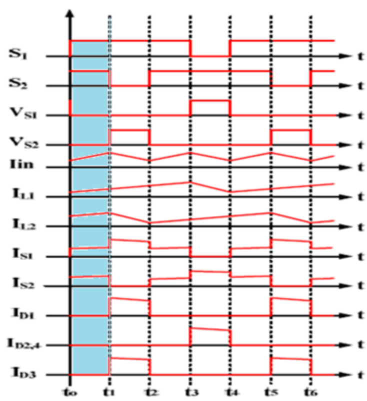


Fig. 2. Mode1 operation **Fig. 3. Theoretical waveforms**

ISSN 2349-7815

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(b). Mode 2[$t_1 - t_3$]:

As shown in figure 4, the switch S_1 is still in the conduction state and the switch S_2 is in the off state. The inductor L_1 still achieves the energy from the input side, so the inductor current i_{L1} is linearly increased. The inductor L_2 is changed to the release-energy state to release the energy to the capacitors C_1 and C_3. The inductor current i_{L2} is then decreased linearly. The diodes D_1 and D_3 are in conduction. The rectifier D_2 must sustain the voltage of C_2. The reverse-bias voltage of D_0 is V_o-V_{C3} at this time.

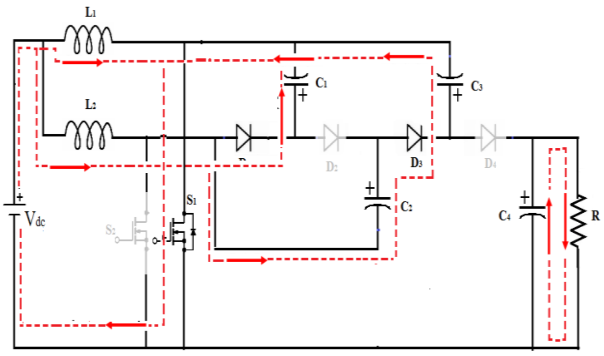

Fig. 4: Mode 2 operation

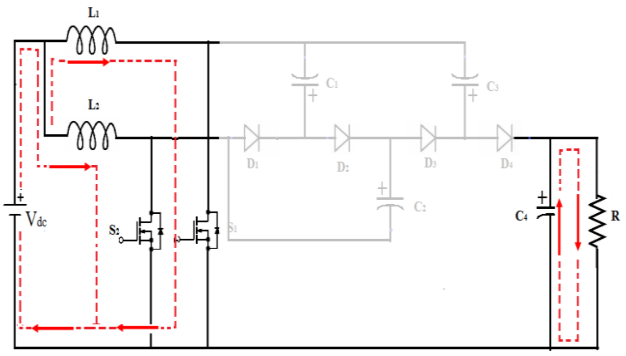

Fig. 5: Mode 3 operation

(c). Mode 3[$t_3 - t_4$]:

As shown in figure 5, the switches S_1 and S_2 are both in conduction. The operation is the same with that of mode 1. All diodes are in the off state. The rectifier D_1 must sustain the voltage of C_1. The rectifiers D_2, D_3, and D_0 must sustain the voltage difference between the before-capacitor and the after-capacitor of their positions.

(d). Mode 4[$t_4 - t_5$]:

As shown in figure 6, the switch S_1 is turned off and the switch S_2 is still in conduction. The inductor L_2 stores the energy so that the inductor current i_{L2} is linearly increased. The inductor L_1 is in the release-energy state. One release-energy path is to release the energy to the C_2 accompanying with the energy of C_1. The other path is to release the energy to the output capacitor accompanying with the energy of C_3. The rectifier diodes D_2 and D_0 are in conduction and the rectifier diodes D_1 and D_3 sustain one-half of the output voltage until to the end of this mode.

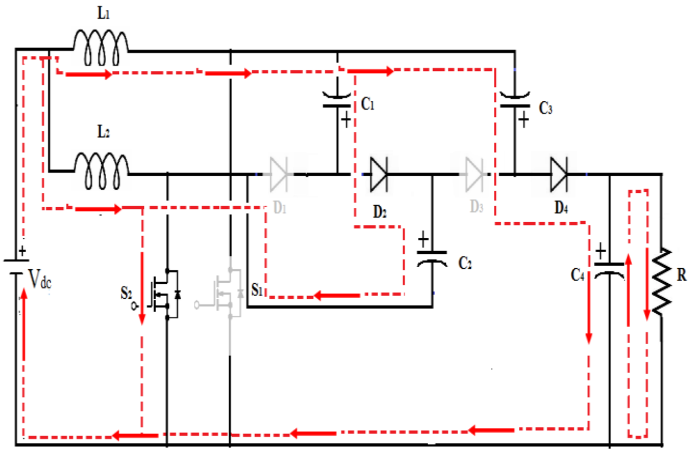

Fig .6: Mode 4 operation

III. SIMULATION MODEL AND RESULTS

In order to verify the operation principle and the theoretical analysis, a converter is simulated with MATLAB/SIMULINK simulation software and the simulation parameters are listed in Table.1. All switches using in simulation are ideal switches. Switching frequency is 60 kHz. Duty ratio is found as 0.72 from the analysis of the converter.

ISSN 2349-7815

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Table I: Simulation parameters

PARAMETERS	VALUES
Input voltage	24V
Output voltage	332V
Switching frequency	60kHz
Duty cycle	72%
Boost inductors (L_1 & L_2)	218μH
Boost capacitors (C_1, C_2, C_3)	220μF
Output capacitor (C_o)	220μF

A. *Control Strategy:*

Control pulses for switch are generated by PWM method. Usually it is done by comparing a saw tooth carrier and a reference value. A repeating sequence of required frequency is compared with a constant 0.45, the duty ratio to generate a pulse with 35% ON time. Whenever repeating sequence is less than the constant, it will output a high value and if constant is smaller, it will output a low value. By varying the value of constant, duty ratio of MOSFET can be controlled. Out of four, two switches have same switching instants and remaining two have the same instants. Two pulses with 180 degree phase shifting is generated by the method of logical operations. Pulse output from the logic circuit is shown in Fig. 7. The first pulse has a phase delay of zero and second pulse is a 180˚ phase shifted.

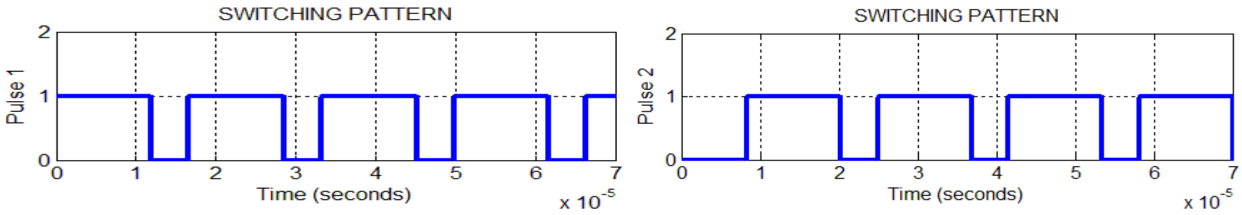

Fig. 7: Pulse output from logical circuit

B. *Simulink Model:*

Simulink model of step up high gain converter is shown in fig. 8. MOSFET's are used as switches. Output voltage and stresses across switches are analyzed from the simulation results.

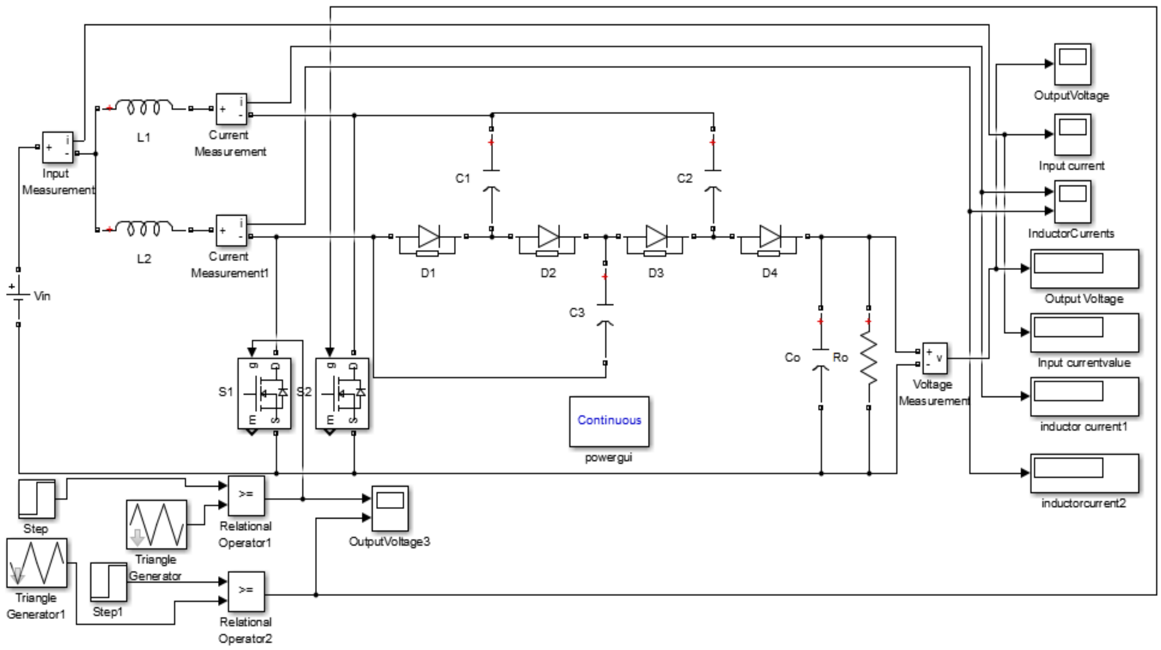

Fig. 8: Simulink model

ISSN 2349-7815

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C. ***Simulation Results:***

Fig. 9(a, b) shows the simulation results at the input voltage 24V. Interleaved boost converter is designed for 24 V input, 350 V output with switching frequency of 60 kHz and duty cycle 72%. Output power is assumed as 150 W. The simulated waveform of switching waveform, source current, voltage stress across the switch, output voltage and current are shown in simulation results. The input current contains a ripple of 0.8 A and the voltage stress is 4 times reduced as that of output voltage.

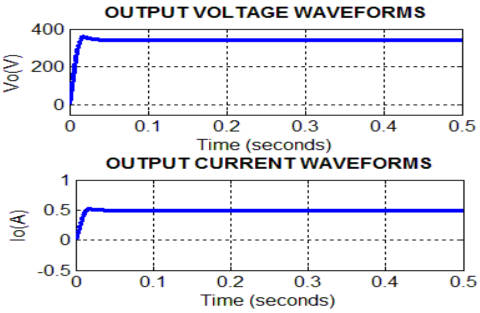

Fig. 9(a): Output voltage (V_O) and output current (Io)

Figure 10 shows the source current and inductor currents for interleaved boost converter with CVU. The voltage impressed across the inductor during the on period of switch is V_{in}. During this period current rises linearly from a minimum level I_{min} to a maximum level I_{max}. The voltage impressed across the inductor during OFF period is V_{out}-V_{in} and current drops linearly from the maximum level I_{max} to minimum level I_{min}. The sum of inductor current will be the source current.

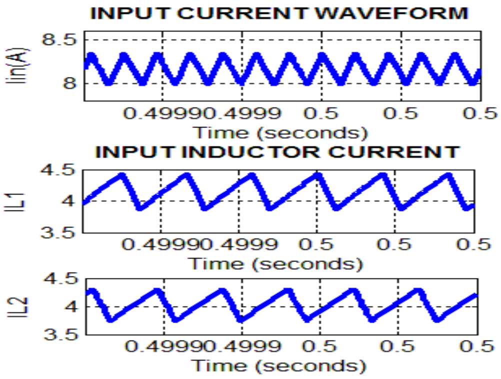

Fig. 10: Source current and inductor currents

It is evident from the simulation result that voltage across switch 1 is zero when the switch S_1 is ON for a time period of 72% and voltage across switch S_1 is 4times less than output voltage when S_1 is OFF. Waveform for voltage across switch S_2 is similar to that of S_1 but is 180˚ phase shifted. Figure 11 shows the voltage waveform across MOSFET.

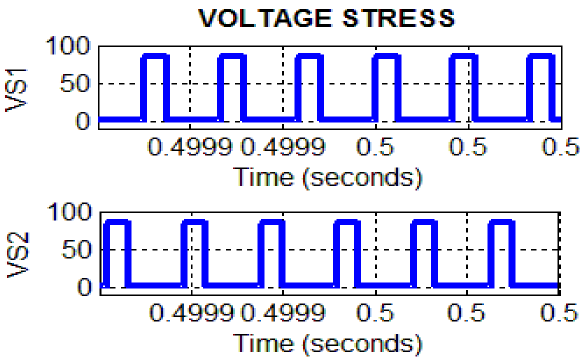

Fig. 11: Voltage stress (VS1 and VS2)

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The Figure 12 shows the variation of Output voltage with respect to duty cycle of the three converter topologies. Voltage gain increases linearly with duty cycle. But gain is improved in IBC with VCU and Figure 13 shows the variation of the voltage gain according to the duty cycle and Figure 14 shows the variation of the voltage stress with respect to the duty cycle. Voltage stress is 4 times reduced in IBC with VCU.

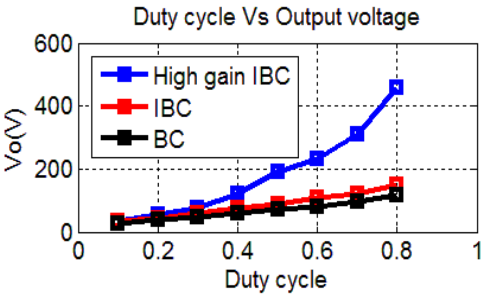

Fig. 12: Output voltage at different duty cycle

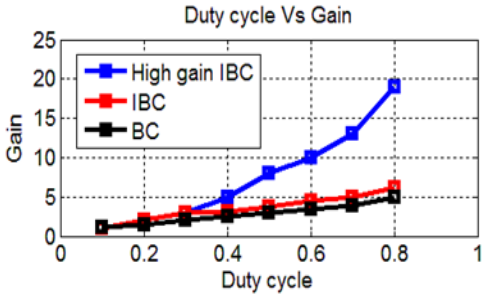

Fig. 13: Gain at different duty cycle

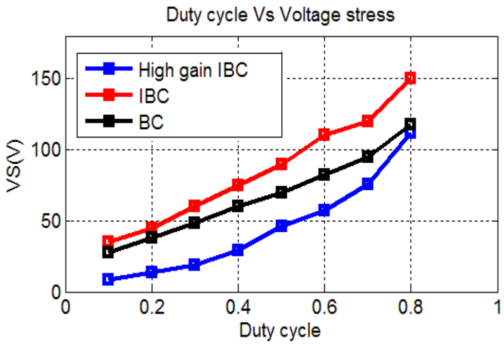

Fig. 14: Voltage stress at different duty cycle

IV. COMPARATIVE STUDY

By modifying conventional boost converter to interleaved boost converter with CVU topology, the voltage stress has reduced to 85 V which is a remarkable advantage compared to existing conventional boost converters (332 V). That is voltage stress is reduced by 74%. Further the efficiency is not sacrificed in order to reduce input current ripple. The input ripple current is reduced by 60%. Table 2 shows the comparative study of interleaved boost converter (CVU) with conventional boost converter and interleaved boost converter.

Table 2: Comparative Study

Parameters	BC	IBC	IBC with VCU
Voltage conversion ratio	1/(1-D)	1/(1-D)	4/(1-D)
Duty cycle	72%	72%	72%
Voltage gain	4.08	5	14.58
Voltage stress	V_O(98 V)	V_O(120 V)	V_O\4(85 V)
Input current ripple	1.4 A	1 A	0.4 A
No. of components	4	7	12
Output power	14W	20W	164W

V. CONCLUSIONS

The modified circuit based on interleaved technique and voltage cumulative unit helps in current sharing capability can reduce the conduction loss of the components and helps to use the smaller inductors. It helps to provide same output voltage as that of conventional converters without using extreme values of duty cycle. The input current ripple is reduced by 33% compared to conventional boost converter. The CVU circuit is used to make up the high step-up dc-dc converter. The CVU circuits can share the common diodes effectively to reduce the number of the diodes and can also increase the

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voltage gain. The voltage stresses of the rectifier diodes and switches are all smaller than the output voltage and they have the clamping effect. The voltage stress across the switches are reduced by 74%. Therefore, the components with smaller rating and lower conduction resistance can be chosen to increase the effeciency of the circuit. The simulation results are verified.

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